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# Evaluation of Polyimide Gate Insulators of Pentacene Organic Thin Film Transistors

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*Thin film organic transistors with $Si/SiO_2$ (300 nm)/pentacene (70 nm)/Au and Si/polyimide (320–690 nm)/pentacene (70 nm)/Au structures have been fabricated and their performances have been compared. The evaluated mobility of the holes of the $SiO_2$ transistor was 0.002 $cm^2/Vs$, while those of the polyimide transistors were between 0.026–0.031 $cm^2/Vs$. On the other hand, the threshold voltage of the $SiO_2$ transistor was $-15$ V, while the threshold voltages of the polyimide transistors were approximately $+4$ V independent of the polyimide thickness. This apparently strange behavior of the polyimide transistors might be attributed to some more negatively charged species accumulating at the polyimide/pentacene interface as the thickness of the polyimide film increases. The PI films had a significantly low level of the leakage current, and the estimated gate-drain leakage current of the corresponding transistor at the gate voltage of $-100$ V is estimated to be negligibly small compared with the source-drain current.*

**Keywords:** gate insulator; organic thin film transistor; pentacene, polyimide

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## 1. INTRODUCTION

Organic transistors have many advantages, large area fabrication, flexible circuitry, and low cost [1–4]. Recently the performance of organic thin film transistors (OTFTs) has improved considerably, and the field effect mobility of OTFTs is now comparable to that of amorphous silicon devices [5]. Consequently, researches have begun on applications of OTFTs to devices such as flexible displays [4], sensors [2], RF tags and smart cards.

In previous studies, $SiO_2$ has been used for the gate insulators of OTFTs [6,7]. However, $SiO_2$ on Si is not flexible, and for further applications of OTFTs, especially for flexible circuits, flexible gate insulators are under development [8,9]. A potentially serious impediment to the performance of flexible gate insulators is residues on the organic films from their fabrication with solutions. To assess this problem we have fabricated OTFTs with organic gate insulators of polyimide (PI) and evaluated the performance of the gate insulators, such as the leakage current and breakdown voltage.

## 2. EXPERIMENTS

### 2.1. Fabrication of Pentacene Transistors

Figure 1 is a schematic of the organic thin film transistors we fabricated. Two kinds of gate insulators, thermally grown $SiO_2$ films and spin coated polyimide on heavily-doped n-type silicon wafer, were prepared. The thickness of the $SiO_2$ was 300 nm, and those of the polyimide were 320 nm, 520 nm, and 690 nm, respectively. The polyimide

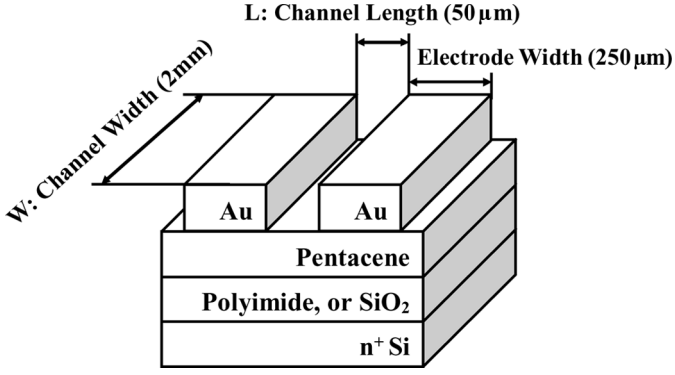
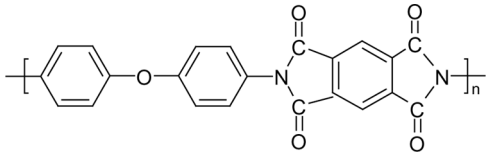



**FIGURE 1** Schematic of the fabricated transistors.

was LX-5800-6, Hitachi Chemical DuPont Micro Systems, Ltd., with the following molecular structure;



The PI solution was dropped and spin-coated on a heavily P-doped Si ($n^+$Si) substrate with a resistivity less than 0.02 Ωcm, and the spin-coating rotation speeds are 800 rpm for 8 seconds and 6000 rpm for 30 seconds. After the spin-coating, the $n^+$ Si substrates with the PI films were cured at 140°C for 2 min., 200°C for 30 min., and 350°C for 60 min. successively on a hot-plate. The thickness of the PI was controlled by varying the spin-coating speed (see Fig. 2) and measured using Ellipsometry. The relative dielectric constant of the PI film was estimated to be approximately 3.4 through capacitance measurements.

After these gate insulators were formed, the pentacene ($C_{22}H_{14}$) films for the semiconductor layers were deposited by thermal vacuum

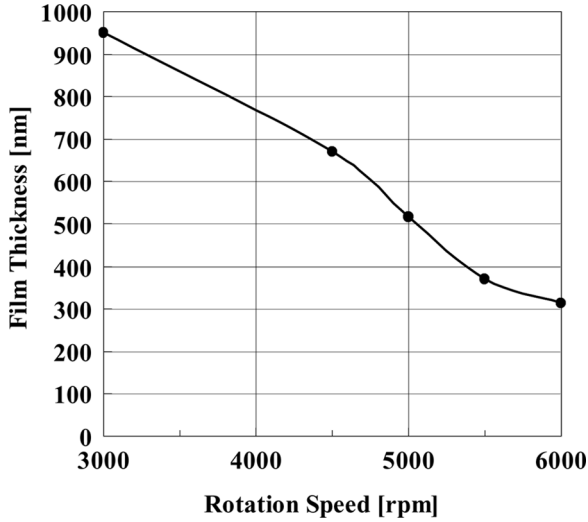
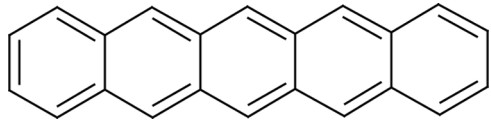



**FIGURE 2** Dependence of the polyimide thickness on the final spin-rotation speed. Note that the thickness is controlled only by changing the final rotation speed.

evaporation at an estimated deposition rate of 0.2 nm/s. The vacuum pressure before the pentacene deposition was usually below $10^{-3}$ Pa. The pentacene was purchased from Wako Pure Chemical Industries, Ltd., and used without further purification. The molecular structure of the pentacene is as follows;



Then, gold was thermally evaporated through a shadow mask to define the source and drain contacts. The defined channel length L and width W were 50 μm and 2 mm, respectively. Please note that the surface of the $SiO_2$ prior to pentacene deposition received no special treatment.

The dependence of the drain current $I_D$was measured as a function of the drain-source voltage, $V_{DS}$, in air using a Semiconductor Parameter Analyzer (Hewlett Packard, Model 4145A).

## 2.2. Fabrication of Metal/Insulator/$n^+$ Si Capacitors and Characterizations

We also fabricated metal/insulator/$n^+$ Si capacitors (insulator: $SiO_2$, PI) to evaluate the leakage current and breakdown characteristics of the PI and $SiO_2$ gate insulators. The capacitor structure is illustrated in Figure 3. The area of the metal electrode was 250 μm × 2 mm, and

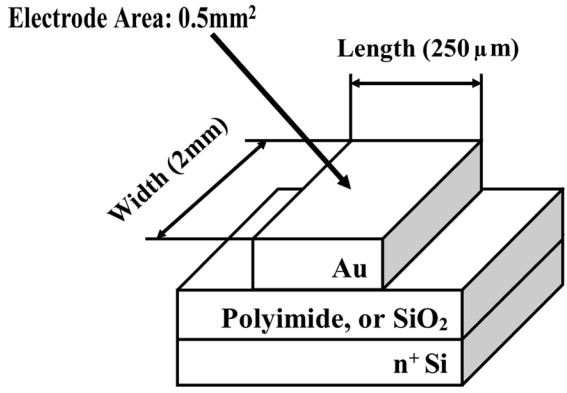



**FIGURE 3** Schematic of metal/insulator/$n^+$ Si capacitor.

the leakage current density is derived from deviding the measured leakage current by the capacitor area. In this case, no pentacene was deposited to evaluate the performance of the gate insulator.

## 3. RESULTS AND DISCUSSION

Figure 4 shows the $I_D$-$V_{DS}$ characteristics of the OTFT with the $SiO_2$ gate insulator. As seen in the figure, a p-type field-effect-transistor operation is obtained for $V_{DS}$ and gate voltages between 0 V to −100 V.

Figures 5 and 6 give the transistor characteristics of the 690 and 320 nm-thick PI transistors, respectively. Note that the drain current $I_D$ of the 320 nm-thick PI transistor is approximately one order of magnitude larger than that of the $SiO_2$ transistor, and that the thinner the PI thickness, the larger the drain current $I_D$.

Figure 7 shows the gate-source voltage dependence of the square root of the drain current. Please note that the extrapolated threshold voltage, $V_{Th}$, of the $SiO_2$ transistor is approximately −15 V, and, curiously, the threshold voltages of the three kinds of PI transistors are

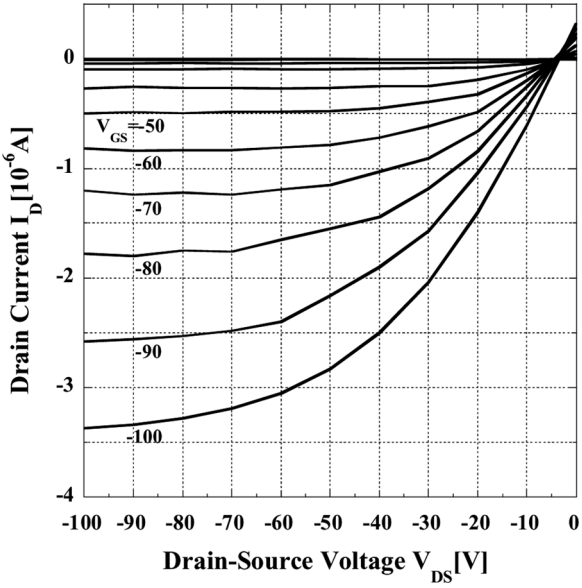



**FIGURE 4** $I_D$-$V_{DS}$ characteristics of the transistor with a 300 nm-thick $SiO_2$ gate insulator.

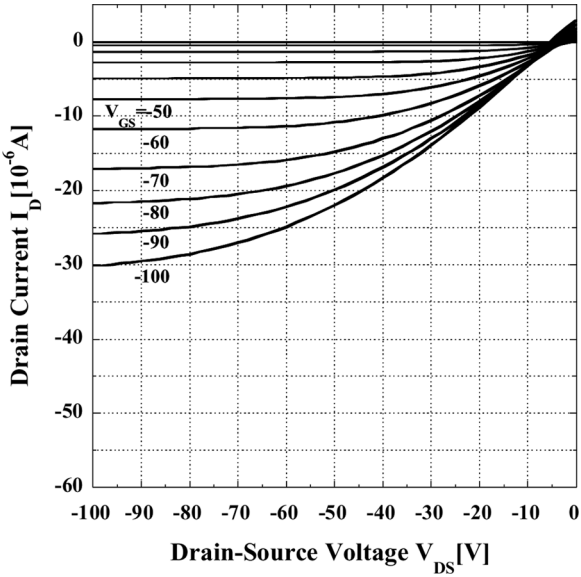



**FIGURE 5** $I_D$-$V_{DS}$ characteristics of the transistor with a 690 nm-thick polyimide gate insulator.

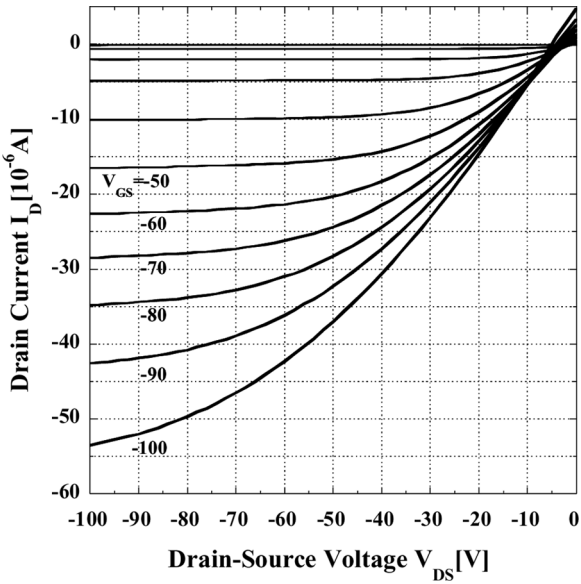



**FIGURE 6** $I_D$-$V_{DS}$ characteristics of the transistor with a 320 nm-thick polyimide gate insulator.

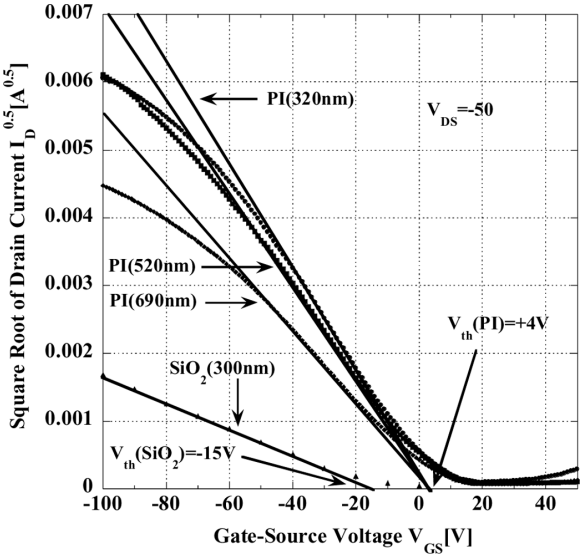



**FIGURE 7** Dependence of the square root of the drain current on the gate-source voltage. Note that the extrapolated voltage for a zero drain current corresponds to the threshold voltage.

all approximately +4V, seemingly independent of the PI thickness. From these curves we also estimated the field-effect mobility of each OTFT using $I_D = WC_i\mu/2L(V_{GS} - V_{Th})^2$ where $W$, $L$, $C_i$, $\mu$, $V_{GS}$, $V_{Th}$ are the channel width, channel length, gate capacitance per unit area, carrier mobility, gate-source voltage, and threshold voltage, respectively [10]. The derived hole mobilities and threshold voltages are summarized in Table 1. The mobility of the $SiO_2$ transistor is only $0.002\,cm^2/Vs$, and the $V_{Th}$ is $-15\,V$. On the other hand, for the PI transistors the mobilities are between 0.026 to $0.031\,cm^2/Vs$. Typically, the absolute value of the threshold voltage of a PI transistor increases as the PI gate insulator thickness increases. However,

**TABLE 1** Comparison of the Mobility and Threshold Voltages of the Fabricated Transistors

| | Mobility [$cm^2$/Vs] | Threshold voltage [V] |
|---|---|---|
| $SiO_2$ 300 nm | 0.002 | −15 |
| Polyimide 690 nm | 0.029 | +4 |
| Polyimide 520 nm | 0.031 | +4 |
| Polyimide 320 nm | 0.026 | +4 |

surprisingly, the $V_{Th}$ for the PI transistors are all $+4\,V$ regardless of the PI thickness. Presently, we do not have any good explanation for this strange phenomenon, but a possible cause could be that there exists negatively-charged chemical species at the PI/pentacene interface and that the amount of this species increases as the thickness of the PI increases.

Finally, we estimated the leakage current level of the gate insulators using the capacitor shown in Figure 3. Figure 8 shows the gate voltage dependence of the leakage current density for the $SiO_2$ and the two PI insulators. Clearly, the leakage-current density levels of the PI gate insulators are much smaller than that of the $SiO_2$ film. The leakage curve of the $SiO_2$ structure is quite flat. Usually a $SiO_2$ diode has a low level of leakage current. This relatively high level of leakage might be due to surface contamination by water. The leakage current densities of the capacitors with the 300 nm $SiO_2$, 690 nm PI, and 320 nm PI at a gate voltage of $-100\,V$ are $8.7 \times 10^{-7}\,A/cm^2$, $2.5 \times 10^{-6}\,A/cm^2$, and $2 \times 10^{-4}\,A/cm^2$, respectively. Therefore, the gate-drain leakage current levels of the fabricated transistors with the 300 nm-thick $SiO_2$, 690 nm-thick PI, and 320 nm-thick PI with the source and drain areas of $250\,\mu m \times 2\,mm$ are estimated to be $-4.3 \times 10^{-9}\,A$, $-1.3 \times 10^{-8}\,A$, and $-9.13 \times 10^{-7}\,A$, respectively (see

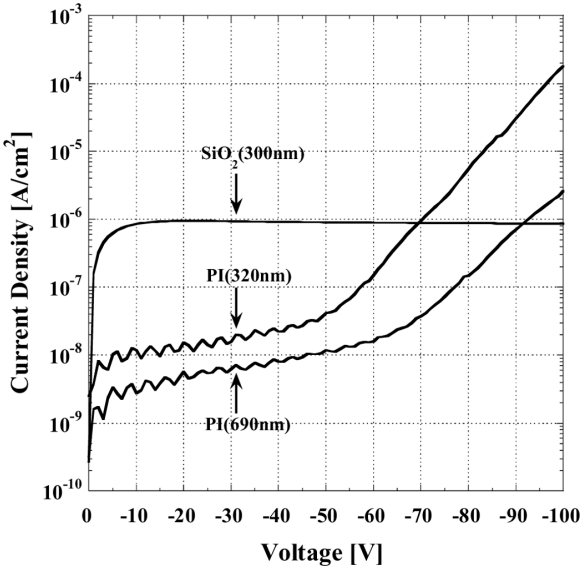



**FIGURE 8** *I-V* characteristics of metal/insulator/$n^+$ Si (insulator: 320 nm-thick PI, 690 nm-thick PI, and 300 nm-thick $SiO_2$)

Fig. 1). In any case the leakage current levels at the gate voltage −100 V are nearly two orders of magnitude lower than the drain current levels (see figure 6, the drain current at the gate bias of $-100\,\mathrm{V}$ is approximately $5.3 \times 10^{-5}\,\mathrm{A}$). Thus, the leakage current through the gate insulators is negligibly small at the gate voltage level of −100 V, within the gate insulator thickness range of the experiments.

## 4. CONCLUSION

Thin film organic transistors with $Si/SiO_2$ (300 nm)/pentacene (70 nm)/Au and Si/polyimide (320–690 nm)/pentacene (70 nm)/Au structures have been fabricated, and their performances compared. The evaluated mobility of the holes of the $SiO_2$ transistor was $0.002\,\mathrm{cm}^2/\mathrm{Vs}$, while those of the polyimide transistors were between $0.026$–$0.031\,\mathrm{cm}^2/\mathrm{Vs}$. On the other hand, the threshold voltage of the $SiO_2$ transistor was $-15\mathrm{V}$, while the threshold voltages of the polyimide transistors were approximately $+4\,\mathrm{V}$ independent of the polyimide thickness. This apparently strange behavior of the polyimide transistors might be attributed to some more negatively charged species accumulating at the polyimide/pentacene interface as the thickness of the polyimide film increases.

The PI films had a significantly low level of the leakage current, and the estimated gate-drain leakage current of the corresponding transistor at the gate voltage of $-100\,\mathrm{V}$ is estimated to be negligibly small compared with the source-drain current.

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